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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/825,646	04/15/2004	Kyoung-Hoi Koo	5649-1297	9472

20792 7590 07/15/2005

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EXAMINER	
TAN, VIBOL	

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 07/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/825,646	KOO, KYOUNG-HOI	
	Examiner	Art Unit	
	Vibol Tan	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 April 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14 and 17-30* is/are rejected.

7)☒ Claim(s) *15 and 16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 2 is objected to because of the following informalities: last line of claim 2, "...less than a logic high..." should be "... less than the logic high..." to avoid lacking of antecedent basis. Appropriate correction is required.

2. In claims 2-21 and 23-30, change "An input..." to "The input..."

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-14 and 17-30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ting et al. (U. S. PAT. 6,198,340) in view of applicant's admitted prior art in Fig. 9.

In claim 1, Ting et al. teaches all claimed features in Fig. 1b, an input circuit for an integrated circuit device, the input circuit comprising: a boosting circuit (14) configured to receive a supply voltage (inherent) of the integrated circuit device and to generate a boosted voltage higher than the supply voltage (Booster 14 is used to boost a voltage); a protection circuit (23) configured to receive an input signal (an input from node 11) and the boosted voltage (from 14 via 15) and to generate an output signal (13) that changes responsive to changes (from logic 0 to logic 1 or vise versa) in the input signal; with the exception of teaching a buffer circuit configured to generate a buffered

output signal responsive to the output signal generated by the protection circuit. However, it is well known in the art to place a buffer such an inverter at the end of a circuit to buffer the output signal as shown in the applicant's admitted prior art in Fig. 9.

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to add a buffer circuit to the end of Ting et al.'s input circuit in order to delay and/or invert the output signal to satisfy design need.

In claim 2, the applicant's admitted prior art in Fig. 9 further teaches the input circuit according to Claim 1 wherein the protection circuit (ANM1) is configured to generate a logic high voltage level output (logic 1 at N2) responsive to a logic high voltage level (INPUT SIGNAL is 4.5-5.5V) of the input signal, wherein the protection circuit is configured to generate a logic low voltage level output (logic 0 at N2) responsive to a logic low voltage level (INPUT SIGNAL is 0V) of the input signal, and wherein the logic high voltage level output (1.3-1.8V) of the protection circuit is less than the logic high voltage level of the input signal (4.5-5.5V).

In claim 3, the applicant's admitted prior art in Fig. 9 further teaches the input circuit according to Claim 1 wherein a logic high voltage level of the output signal (1.3-1.8V) is less than a logic high voltage level of the input signal (4.5-5.5V).

In claim 4, Ting et al. further teaches in Fig. 1b the input circuit according to Claim 3 wherein the protection circuit (23) comprises a MOS transistor having a gate coupled to the boosted voltage (14, 15) and a first source/drain coupled to the input signal (node 11), wherein the output signal is generated at a second source/drain of the MOS transistor (13), and wherein high voltage level of the output signal is approximately

a difference 3Vcc – threshold voltage of transistor 23) between the boosted voltage and a threshold voltage of the MOS transistor.

In claim 5, Ting et al. further teaches the input circuit according to Claim 1 wherein the boosting circuit is configured to generate the boosted voltage having a voltage approximately two times higher than the supply voltage (2Vcc; vol. 3, line 31).

In claim 6, Ting et al. further teaches the input circuit according to Claim 1 wherein the boosting circuit comprises a charge pump (1b is a pump circuit).

Claim 7 corresponds to detailed circuitry already discussed similarly with regard to claim 4.

In claim 8, the applicant's admitted prior art in Fig. 9 further teaches the input circuit according to Claim 1 wherein the buffer circuit includes first and second serially coupled switching circuits (AP2, ANM2 and an end inverter), wherein the first switching circuit (AP2, ANM2) inverts the output signal generated by the protection circuit (ANM1) and wherein the second switching circuit (the end inverter) inverts the output of the first switching circuit to generate the buffered output signal.

In claim 9, the applicant's admitted prior art in Fig. 9 further teaches the input circuit according to Claim 8 wherein the first switching circuit comprises first and second transistors (AP2 and ANM2) serially coupled between the supply voltage (V_{DD} via AP1) and ground.

In claims 10 and 11, it is obvious to employ two serially connected transistors for the second switching, as taught in the first switching circuit of the applicant's admitted prior art in Fig. 9, and it is well known in the art.

Claims 12-14 are rejected in the same manner as claims 8-11.

In claims 17 and 18, Ting et al. further teaches the input circuit according to Claim 1 wherein the protection circuit comprises a pass transistor (23) having a gate coupled to the boosted voltage of the boosting circuit (14, 15), a first source/drain coupled to the input signal (at node 11), and a second source/drain (13) coupled to the buffer circuit (not shown); and wherein the pass transistor (23) comprises an NMOS transistor.

In claim 19, the applicant's admitted prior art in Fig. 9 further teaches the input circuit according to Claim 1 wherein a logic high voltage level of the input signal is greater than approximately 4.5 volts (4.5-5.5V) and wherein the supply voltage of the integrated circuit device is less than approximately 2 volts (V_{DD}; 1.3-18V).

In claim 20, the applicant's admitted prior art in Fig. 9 further teaches the input circuit according to Claim 1 wherein the buffer circuit comprises two serially coupled inverters (AP2, ANM2 and an end inverter).

In claim 21, the applicant's admitted prior art in Fig. 9 further teaches the input circuit according to Claim 1 wherein a logic high voltage level of the buffered output signal at N2) is less than approximately 2 volts (1.8V).

Method claims 22-30 correspond to detailed circuitry already discussed similarly with regard to claims 1-14 and 17-21.

5. Claims 15 and 16 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (571) 272-1769. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VIBOL TAN
PRIMARY EXAMINER